Active Doubler
7.5 - 25.0 / 15.0 - 50.0 GHz

Features

- Excellent Broadband Mixer Driver
- Single Ended Fed Doubler with Distributed Buffer Amplifier
- Excellent LO Driver for MACOM Receivers
- +15 dBm Output Drive
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010
- RoHS* Compliant

Applications

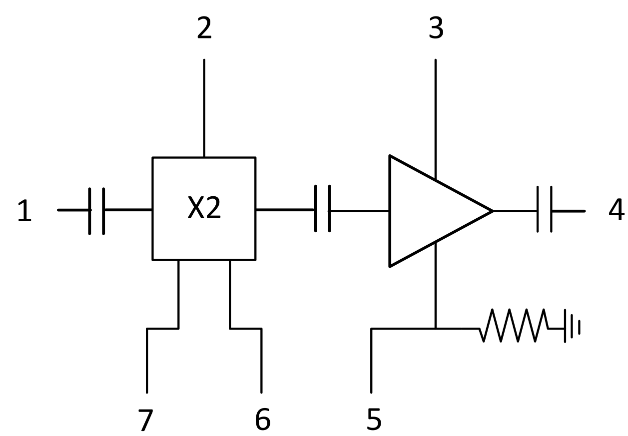
- Point-to-Point Radio
- Microwave
- LMDS
- SATCOM
- VSAT

Description

This single ended fed (no external balun required) 7.5 - 25.0 / 15.0 - 50.0 GHz GaAs MMIC doubler has a 15 dBm output drive and is an excellent LO doubler that can be used to drive fundamental mixer devices. It is also well suited to drive MACOMs' XR1002 receiver device.

This MMIC uses a GaAs pHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process.

Functional Block Diagram



Pad Configuration[1]

Pad	Function	Description
1	RF_{IN}	RF Input
2	V_D1	Drain Voltage Stage 1
3	V_D2	Drain Voltage Stage 2
4	RF_{OUT}	RF Output
5	V_G2	Gate Voltage Stage 2
6	V_{SS}	Source Supply Voltage
7	V_G1	Gate Voltage Stage 1

1. Backside metal is RF, DC and thermal ground.

Ordering Information

Part Number	Package
XX1000-BD-000V	vacuum release gel paks
XX1000-BD-EV1	evaluation board

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: Input Freq. = 7.5 - 25 GHz, T_A = 25°C

Parameter	Units	Min.	Typ.	Max.
Output Frequency Range	GHz	15	—	50
Input Return Loss	dB	—	12	—
Output Return Loss	dB	—	12	—
Harmonic Gain	dB	—	13	—
Fundamental Rejection	dBc	—	20	—
Saturated Output Power	dBm	—	15	—
RF Input Power	dBm	-10	—	+10
Output Power @ 0 dBm P_{IN}	dBm	—	13	—
Drain Bias Voltage (V_D1,2)	VDC	—	5.0	5.5
Gate Bias Voltage (V_G1)	VDC	-1.2	-0.6	+0.1
Gate Bias Voltage (V_G2)	VDC	-1.2	0.0	+0.1
Quiescent Drain Current (I_D1,2) (V_D = 5 V, V_G1 = -0.6 V, V_G = 0 V Typical)[2]	mA	—	210	—
Source Voltage (V_{SS})	VDC	-5.5	-5.0	-2.0
Source Current (I_{SS})	mA	25	50	60

2. Adjust V_G1 to set 70 mA I_{DQ}1, adjust V_G2 to set 140 mA I_{DQ}2.

Absolute Maximum Ratings[3]

Parameter	Absolute Maximum
Drain Voltage (V_D1, V_D2)	+6 V
Source Voltage (V_{SS})	-6 V
Drain Current (I_D1+I_D2)	320 mA
Source Current (I_{SS})	60 mA
Gate Bias Voltage (V_G1)	+0.3 V
Gate Bias Voltage (V_G2)	+0.1 V
RF Input Power	+12 dBm
Storage Temperature	-65°C to +165°C
Operating Temperature	-55°C to MTTF Table
Channel Temperature	MTTF Table

3. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

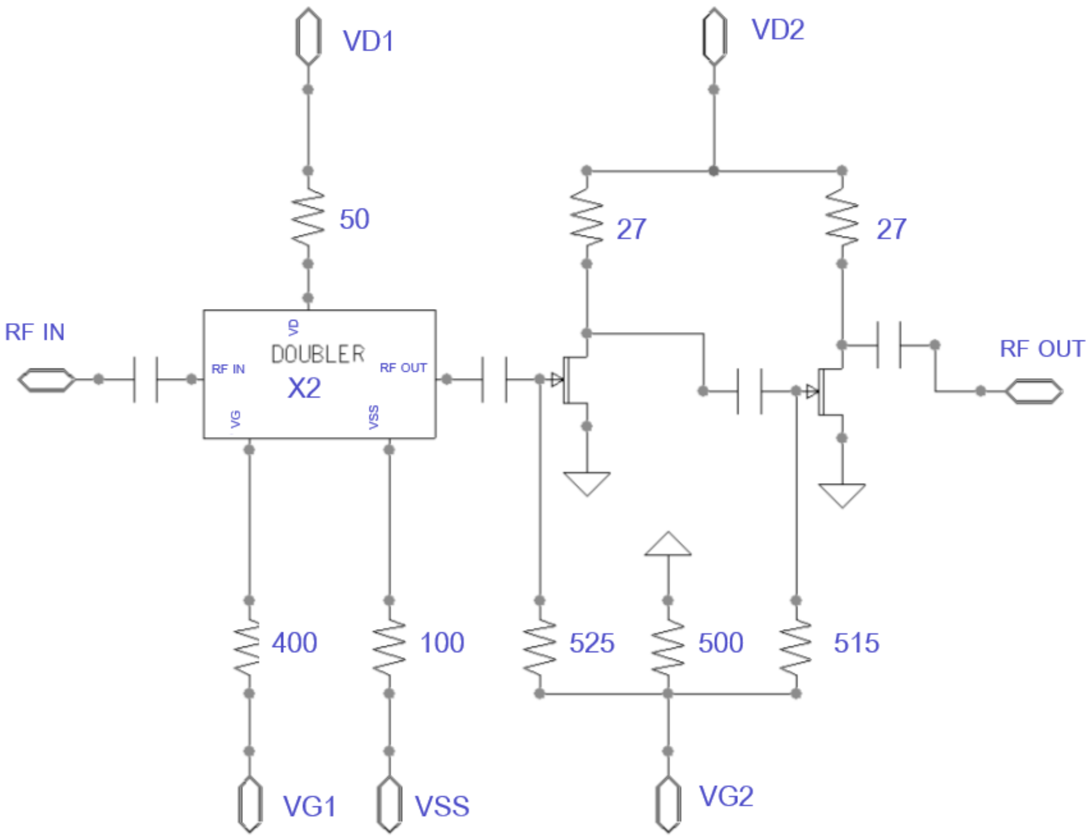
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

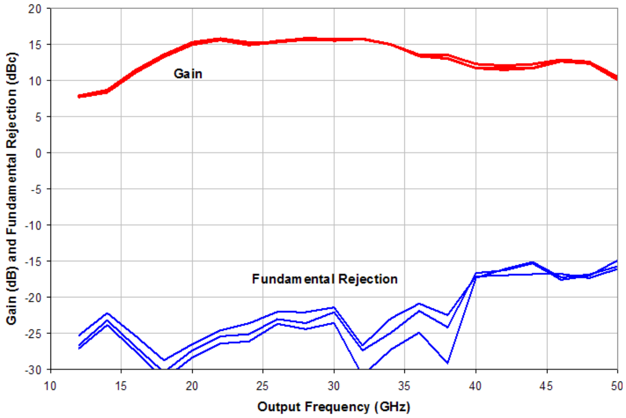
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 2 devices.

Block Diagram & Schematics

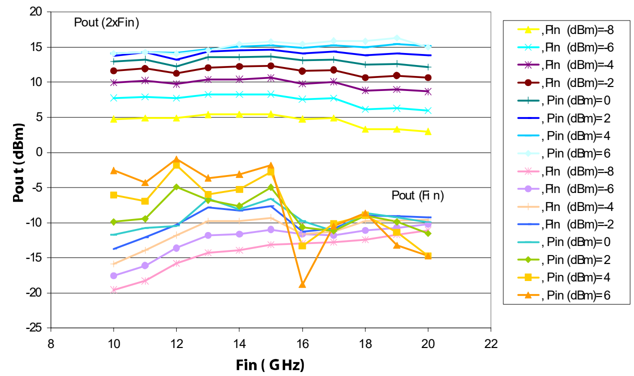


Typical Performance Curves

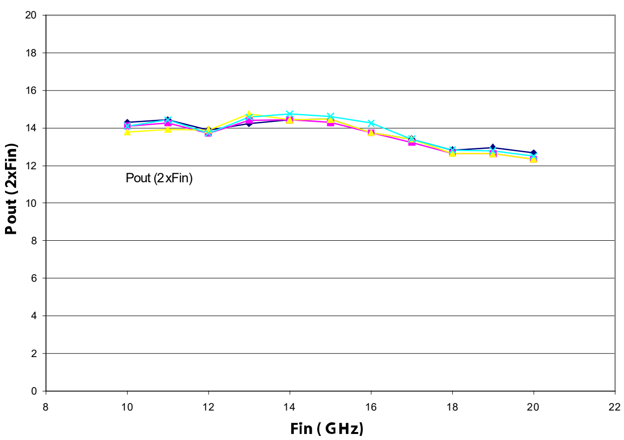
**Harmonic Gain and Fundamental Rejection vs Output Freq.
Pin = 0 dBm**



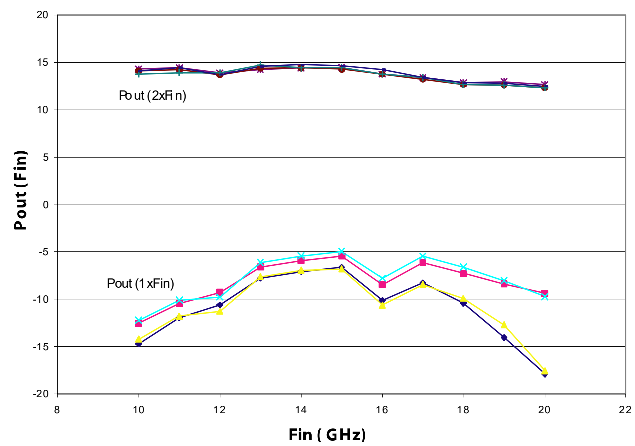
**XX1000-BD: Pout (2xFin) and Pout (Fin) vs. Fin (GHz)
Pin = -8 to +6 dBm**



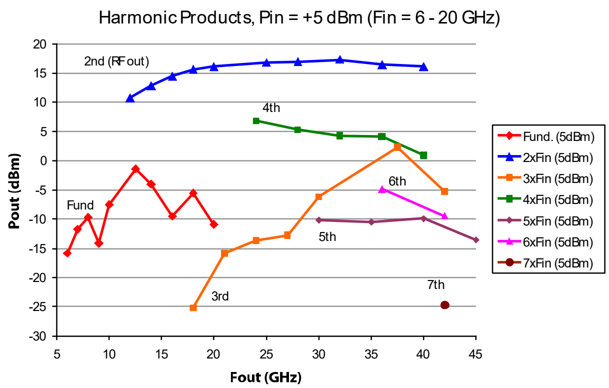
**XX1000-BD_4_samples: Pout (2xFin) vs. Fin (GHz)
Pin=0dBm, VD1=5V, VG1=-0.6V, VSS=-5V, VD2=5V ~150mA, VG2=open**

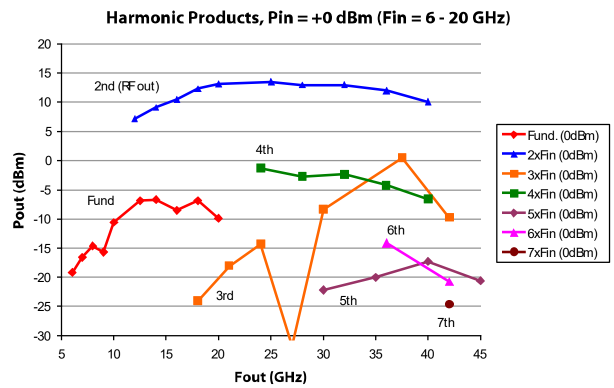


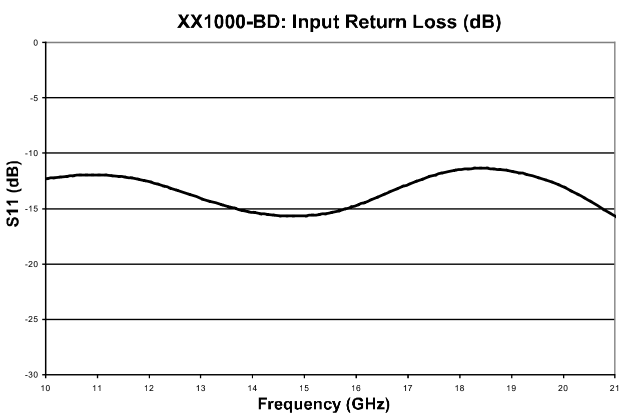
**XX1000-BD_4_samples: Pout (Fin) vs. Fin (GHz)
Pin=0dBm, VD1=5V, VG1=-0.6V, VSS=-5V, VD2=5V ~150mA, VG2=open**



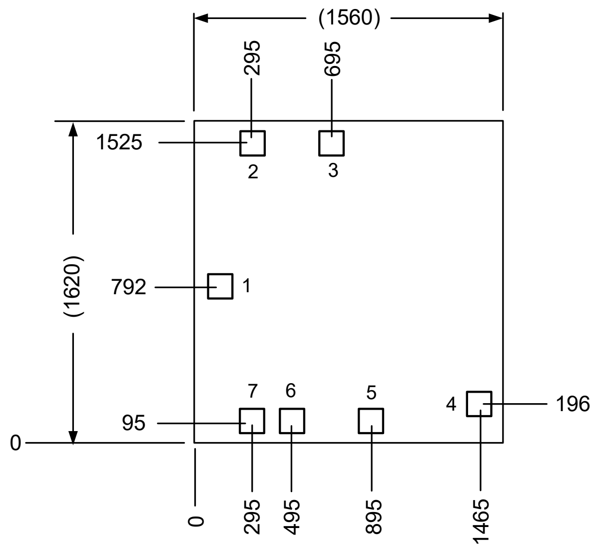
Typical Performance Curves (cont.)



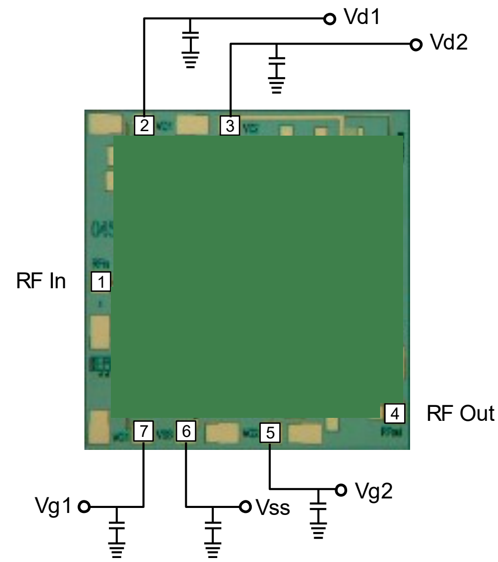




Mechanical Drawing



Bias Arrangement



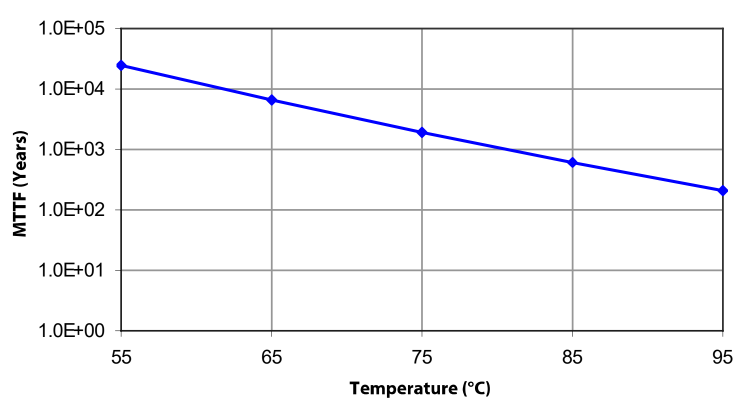
Bypass Capacitors - See App Note [2]

Bond Pad Size (µm)

Pad	X	Y
1 - 7	100	100

Unless otherwise specified, all dimensions are µm with a tolerance of ±5 µm.
Die thickness is 110 ±10 µm.
Bond pad / backside metallization: Gold
Die size reflects final cut dimensions.

MTTF vs. Back-plate Temperature (°C)

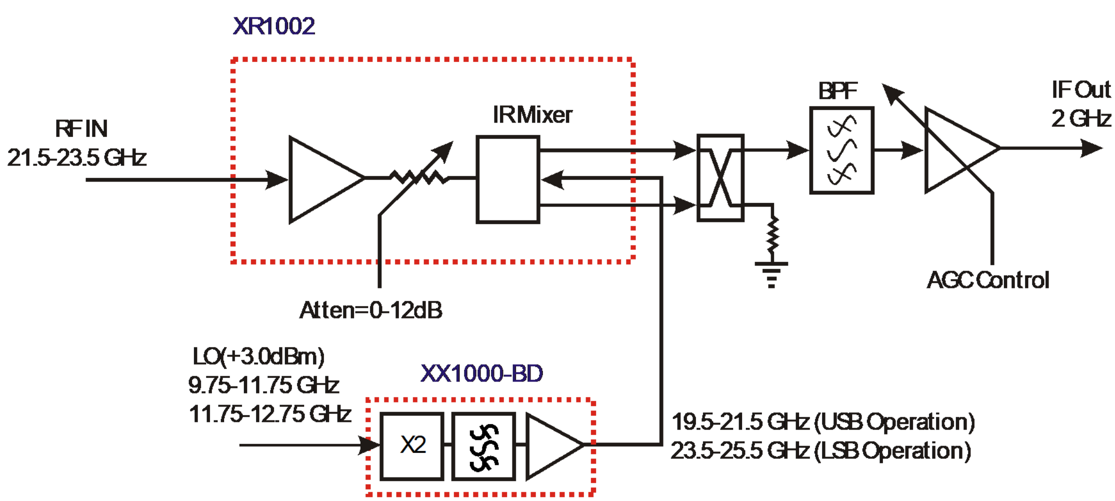


MTTF is calculated from accelerated life-time data of single devices and assumes isothermal back-plate.
Bias Conditions: V_D1,2 = 5 V, I_D1,2 = 220 mA, V_{SS} = -5 V, I_{SS} = 50 mA

App Note [1] Biasing -
It is recommended to separately bias each doubler stage with fixed voltages of $V_D1,2$ = 5 V, V_{SS} = -5 V and V_G1 = -0.6 V. The typical DC currents are I_D1 = 80 mA, I_D2 = 140 mA and I_{SS} = 50 mA. V_G2 can be used for active control biasing of V_D2, or it can be left open and V_D2 will self bias at approximately 140 mA. Maximum output power is achieved with V_{SS} = -5 V and I_{SS} = 50 mA but the device will operate with reduced bias to V_{SS} = -2 V and I_{SS} = 25 mA. It is also recommended to use active biasing on V_D2 with V_G2 to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage for V_G2 = -0.1 V. Typically the gate is protected with silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement -
For individual stage bias (recommended for doubler applications) - Each DC pad ($V_D1,2$, V_{SS} and $V_G1,2$) needs to have DC bypass capacitance (~100 - 200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 µF) is also recommended.

Typical Application



MMIC based 18 - 34 GHz Double / Receiver Block Diagram
(changing LO and IF frequencies as required allows the design to operate as high as 34 GHz.